IN THE SPECIFICATION

Please replace paragraph 0019 with the following:

[0019] Referring now to **FIGURE 1**, there is illustrated a block diagram describing MPEG formatting of video data 305. The video data 305 comprises a series of frames 310. Each frame comprises two dimensional grids of luminance Y, chroma red Cr, and chroma blue Cb pixels ~~315~~. The two-dimensional grids are divided into 8x8 blocks 335, where four blocks 335 of luminance pixels Y are associated with a block 335 of chroma red Cr, and a block 335 of chroma blue Cb pixels. The four blocks of luminance pixels Y, the block of chroma red Cr, and the chroma blue Cb form a data structure known as a macroblock 337. The macroblock 337 also includes additional parameters, including motion vectors.

Please replace paragraph 0020 with the following:

[0020] The macroblocks 337 representing a frame are grouped into different video packets 340. The video packet 340 includes the macroblocks 337 in the video packet 340, as well as additional parameters describing the video packet. Each of the video packets 340 forming the frame form the data portion of a picture structure 345. The picture 345 includes the video packets 340 as well as additional parameters. The pictures are then grouped together as a group of pictures 350. The group of pictures 350 also includes additional parameters. Groups of pictures 350 are then stored, forming what is known as a video elementary stream 355. The video elementary stream 355 is then

packetized to form a packetized elementary stream ~~sequence 360~~. Each packet is then associated with a transport header ~~365a~~, forming what are known as transport packets ~~365b~~.

Please replace paragraph 0021 with the following:

[0021] The transport packets ~~365b~~ can be multiplexed with other transport packets ~~365b~~ carrying other content, such as another video elementary stream 355 or an audio elementary stream. The multiplexed transport packets from what is known as a transport stream. The transport stream is transmitted over a communication medium for decoding and presentation.

Please replace paragraph 0024 with the following:

[0024] The video transport processor 440 converts the video transport stream into a video elementary stream and provides the video elementary stream to an MPEG video decoder 445 that decodes the video. The video elementary stream ~~355~~ is stored in a compressed data buffer (CDB) 447. The MPEG video decoder 445 accesses the compressed data buffer (CDB) to receive the video elementary stream ~~355~~. The video elementary stream ~~355~~ is decoded by the MPEG video decoder 445 resulting in the reconstructed video data 305.

Please replace paragraph 0025 with the following:

[0025] The audio data is sent to the output blocks and the video data ~~305~~ is sent to a display engine 450. The display engine 450 is responsible for and operable to scale the

video picture, render the graphics, and construct the complete display among other functions. Once the display is ready to be presented, it is passed to a video encoder 455 where it is converted to analog video using an internal digital to analog converter (DAC). The digital audio is converted to analog in the audio digital to analog converter (DAC) 465.

Please replace paragraph 0038 with the following:

[0038] The foregoing provides the data words 505(x)...505(n) as a set of 32 bit words starting from the last portion of 505(n) and proceeding sequentially to the first portion of 505(x). The bits forming the 32-bit words can be reversed with respect to one another, in any number of ways. For example, the MPEG video decoder 445 can include logic that reverses the 32 bits of each word. Alternatively, the DMA engine 510 can include additional circuitry 550 that causes the 32 bits of each word 611 to be provided to the MPEG video decoder 445 in the reverse order via port 560.

Please insert the following paragraph after paragraph 0038:

[0038.1] FIGURE 5 is a block diagram describing circuitry 550. The circuitry comprises multiplexers 555(0)…555(31) for providing selectively providing data word 611 via p9ort 560 in either forward or reverse order based on a signal REVERSE.

Please replace paragraph 0039 with the following:

[0026] Referring now to **FIGURE 6** ~~**FIGURE 5**~~, there is illustrated a flow diagram for providing a video packet in a reverse order. At 705, the state logic machine 605 receives a command to fetch data words in an address range, e.g., 505(x)-510(n) from the MPEG video decoder 445, accompanied by a control signal indicating that the data words in the address range are to be provided to the MPEG video decoder 445 in the reverse order, e.g., 505(n), 505(n-1)...505(x).